



**WB32F10x 12Bit ADC
Application Note**

Westberry Technology (ChangZhou) Corp., Ltd

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1 Layout Note

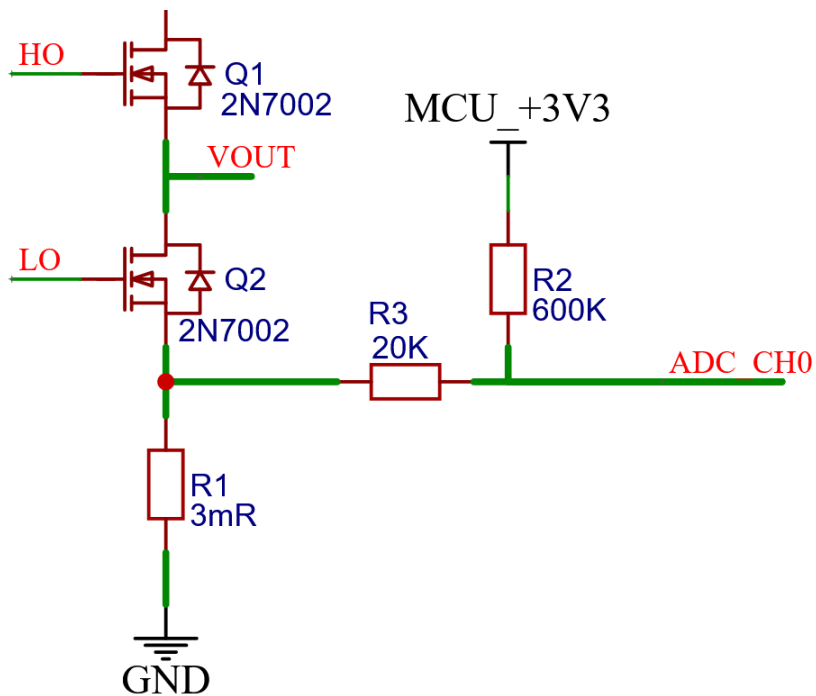
- Use the same power supply to VDD and VDDA, ensure that the dropout voltage between VDD and VDDA is less than 500mV.
- The VDD pins must be connected to VDD with external decoupling capacitors (one 100nF Ceramic capacitor for each VDD pin + one Tantalum capacitor (Min. 4.7 μ F Typ.10 μ F)).
- VDDA pin must be connected to 2 external decoupling capacitors.(10nF Ceramic Capacitor +1 μ F Tantalum).
- Analog channels need to be separated using ground(GND).

2 ADC Programming Note

- After the SARADC is turned on or the working mode is changed, it takes a period of time (100us) to wait for the SARADC to stabilize before starting the conversion.
- Recalibration is required every time the SARADC is turned on.
- The conversion result of the SARADC must be read using the function ADC_GetADValue() in the library.
- It is recommended that the clock frequency of the SARADC is set to 6MHz, and the sampling time is set to 8 SARADC clock cycles.
- Please refer to the example:
[WB32F10x StdPeriph Lib\Project\WB32F10x StdPeriph Examples\ADC](#)

3 Weak Voltage Acquisition Scheme

The problem of ADC sampling weak voltage accuracy can be solved by adding input bias voltage to ADC.



Revision History

Revision	Date	Description
1.0	2020/09/05	Initial Release
1.1	2022/06/30	Added Weak Voltage Acquisition Scheme

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